## REMARKS

Claims 1-21, all the claims pending in the application, stand rejected on prior art grounds. Applicant respectfully traverses this rejection based on the following discussion.

### I. The Prior Art Rejections

Claims 1-21 stand rejected under 35 U.S.C. §103(a) as being unpatentable over Aguilar et al. (U.S. Patent No. 6,199,137), hereinafter referred to as Aguilar in view of Maduzia et al. (U.S. Patent No. 5,488,408), hereinafter referred to as Maduzia. Applicants respectfully traverse these rejections based on the following discussion.

#### A. The §103(a) Rejection Based on Aguilar and Maduzia

Applicant respectfully traverses this rejection because the prior art of record does not disclose selectively engaging different numbers of serial data lanes to alter the speed of data passing through a core and, therefore, such a element is a missing claim element in the rejection. The rejection does not make reference to any teaching of the missing claim element, and instead proposes that the missing claim element would have obviously been added to the structures disclosed by the prior art of record. Thus, the rejection is traversed for two primary reasons, the first reason is that the missing claim element is not shown anywhere in the prior art of record, and the second reason is that the logic for the addition of the missing claim element is not supported by any teaching of record.

The Office Action admits that Aguilar does not disclose selectively engaging serial data lanes to alter the speed of data passing through the core. The Office Action refers to Maduzia only for teaching selecting a number of lines of a serial communication. Then, the Office Action concludes that it would have been obvious to selectively engage the serial data lanes to alter the speed of data passing through the core because the "speed of data transmission depends upon available bandwidth" which is an

unsupported assertion and is potentially incorrect. Therefore, the rejection is defective for two separate reasons. The first reason is that the obviousness rejection does not provide a teaching for each of the claim elements (missing claim element) and the second reason is that the logical basis for the alteration of the references is based upon an unsupported and potentially incorrect assertion.

With respect to the first reason that the rejection is defective, there simply is not any teaching in the prior art of record (nor does the rejection point to any teaching in the prior art of record) of selectively engaging different numbers of serial data lanes in order to alter the speed of data passing through a core. The missing claim element defect is demonstrated, for example, in paragraphs 6 and 7 on page 3 of the rejection where paragraph 6 relates the teachings of the applied prior art references and paragraph 7 draws the conclusion of obviousness stating that the missing claim element would have been an obvious feature to add. Thus, Applicant submits that, because of the missing claim element, the rejection is defective on its face.

An obviousness rejection must demonstrate where each claim element is shown in the prior art references, even if multiple references are being combined with some claim elements been taken from each of the different references. In other words, an obviousness rejection can properly take some of the claim elements from one reference and other claim elements from a different reference and argue that the combined teaching of the two different references teaches all the claim elements. In addition, an obviousness rejection may teach one ordinarily skilled in the art to alter one of the claim elements that is taught by a different reference. However, in either case, all claim elements must be positively discussed in the prior art of record. One of the defects of the present rejection is that the present claims defined an element which the Office Action itself demonstrates is not taught by the prior art of record (that element being the selective engagement of a different number of serial data lanes to alter the speed of data passing through the core). Rather than providing a reference with such a teaching, the rejection merely states that the addition of such an element would have been obvious. Therefore, the rejection is defective on its face even before the prior art is analyzed on its merits because the Office Action does not make reference to a prior art of record for teaching one of the claim elements.

With respect to the second reason that the rejection is defective, the conclusion of obviousness is based upon the unsupported (and potentially incorrect) statement that the "speed of data transmission depends upon available bandwidth." This teaching of a relationship between bandwidth and transmission speed is not supported by any reference in the prior art of record. Indeed, such a statement may not be correct because many devices having a relatively large bandwidth can operate at a relatively slow data transmission speed when compared to higher speed, smaller bandwidth devices (transmission speed of a core connected to a transmission media is dependent upon many factors including different protocols, compression schemes, buffer activity, power arrangements etc., and is not necessarily dependent upon bandwidth). Therefore, even the logical reasoning behind the conclusion of obviousness is unsupported (and even somewhat questionable). That is, not only does the implied prior art of record not teach the claimed element of the selector "selectively engages different numbers of said serial data lanes to alter a speed of data passing through said core" the logical reasoning for the obviousness conclusion appears to be without basis in the prior art of record.

Maduzia discloses a device (a TV channel metering apparatus) that connects to a TV receiver and that can be configured to differently connect to serial lines of a data bus within the TV receiver depending upon to which type of receiver the TV channel metering apparatus is connecting. Maduzia does not teach or suggest any situation or structure where different numbers of serial data lanes can be selectively engaged to alter the speed of data passing through the core as defined by independent claims 1, 8, and 15 where they define that the "selector selectively engages different numbers of said serial data lanes to alter a speed of data passing through said core."

The rejection relies on claims 12 and 16 of Maduzia for teaching that the concept of selecting a number of lines of a serial communication. Claims 12 and 16 utilize means-plus-function language (which requires reference to the specification) and the functions defined by claims 12 and 16 appear to be described in column 9, line 40-column 10, line 5 of the specification of Maduzia which explains Figures 5-7. That portion of Maduzia describes that the TV channel metering equipment is designed to be connected to many different types of commonly available digital TV receivers, each of which can have different bus structures. As described in column 9, line 40-column 10,

line 5 of the specification of Maduzia, the TV channel metering devices can be programmed to match the data communication bus architecture associated with each different type of commonly available digital TV receiver. The Office Action does not propose that Maduzia teaches selectively engaging different numbers of serial data lanes to alter the speed of data passing through a core, because the Office Action only states that Maduzia teaches the concept of selecting a number of lines of a serial communication and the rejection subsequently (for example in paragraph 7 on page 3 of the Office Action).

The rejection does not provide any reference to a teaching of selectively engaging different numbers of serial data lanes of a core that connects a processor to a transmission media in order to alter the speed of data passing through the core. Instead, the rejection refers to a teaching of a router having a fixed number of lanes (Aguilar) and a teaching that a metering device can be adapted to accommodate different bus architectures/structures depending upon what type of receiver the metering device is attached to (Maduzia) before drawing a conclusion of obviousness (based on a questionable and unsupported relationship between transmission speed and bandwidth).

The actual structure that would be produced by the proposed combination of a router having a fixed number of lanes (Aguilar) and a metering device adapted to accommodate different bus architectures/structures (Maduzia) is a router that has a fixed number of lanes that is adapted to connect to various types of different bus architectures/structures. Nothing within such a proposed structure would selectively engaged different numbers of serial data lanes to alter the speed of data passing through the core as is claimed. The rejection proposes that this structure created by the combination of Aguilar and Maduzia would be obvious to further modify; however, as shown above, there is no basis for such a proposed modification.

Therefore, the rejection is defective because it fails to provide a teaching of a claimed element and does not provide support for the obvious addition of such a missing claimed element. Specifically, the rejection does not point to any reference that teaches or suggests "selectively engages different numbers of said serial data lanes to alter a speed of data passing through said core." Here, there simply is no reference which is relied upon for the teaching of selectively engaging "different numbers of said serial data

lanes to alter a speed of data passing through said core." Instead, this element is added as being obvious and the obviousness reasoning is based upon the unsupported statement that the "speed of data transmission depends upon available bandwidth."

Therefore, it is Applicant's position that prior art of record does not teach or suggest the claimed operation where the selector "selectively engages different numbers of said serial data lanes to alter a speed of data passing through said core" as defined by independent claims 1, 8, and 15. As shown in Applicant' Figure 2B, the multiplexers 215, 236 selectively engage a different number of data lanes 225 (e.g., alter the lane width) in order to perform a speed reduction between the transmission media 280 and the ASIC 246. For example, with the exemplary structure shown in FIG. 2B, the invention can perform speed reduction by simultaneously transmitting the data along four lanes.

To illustrate the utility of the invention, given that 12 data lanes are used in a network, when in a 4X reduction mode of operation, physical data lanes 4-11 can be used as wider extensions of lanes 0-3. Further, when in a 1X mode of operation using these 12 data lanes, FIFOs for data lanes 1-11 can be a wider extension of the FIFO used for data lane 0, thereby achieving up to a 12X speed reduction. Thus, when data is accessed at the transmission media 280, by using the multiplexers 215, 236, the upper link layer 250 can access wider data at a slower rate. The invention also produces an advantage in that receive elastic FIFO buffers 220 perform the function of the frequency correction portion 260 and correct any frequency deviations which may occur along the transmission media 280. FIFO buffers 220, 230 also modify the frequency of the signal to that desired by the ASIC 246. Therefore, the FIFO buffers 220 perform the functions that were previously performed by FIFO buffers 251 and 261 shown in FIG. 2A, thereby reducing the number of buffers within the core logic 210. This decrease in the number of buffers within the core logic 210 reduces power consumption, increases processing speed and decreases the chip area consumed by the core logic 210.

To the contrary, as can be seen in Figures 2, 4, and 5 of Aguilar, the Aguilar teaching is limited to a fixed number of serial data lanes which indicates that a mechanism other than a number of engaged serial data lanes controls the data transmission speed. Figures 5-7 of Maduzia utilize a different number of connections between the computer and the various components; however, each example provided in

Figures 5-7 utilize a single data line which similarly indicates that a mechanism other than a number of engaged serial data lanes controls the data transmission speed. Neither of the applied prior art references provide any suggestion for changing the number of serial data lanes that are engaged in order to alter the speed of the data that is being transmitted. There is no logical basis in the prior art of record for altering Aguilar to include a selector that selectively engages serial data lanes to alter data transmission speed as is claimed.

Thus, as shown above, Aguilar does not teach or suggest selectively engaging serial data lanes to alter the data speed and Maduzia also does not teach or suggest this feature. Therefore, the proposed combination of Aguilar and Maduzia does not teach or suggest the claimed operation where the selector "selectively engages different numbers of said serial data lanes to alter a speed of data passing through said core" as defined by independent claims 1, 8, and 15. Therefore, it is Applicant's position that the proposed combination of Aguilar and Maduzia does not render obvious independent claims 1, 8, and 15 and that such claims are patentable over the prior art of record. Further, dependent claims 2-7, 9-14, and 16-21 are similarly patentable, not only by virtue of their dependency from a patentable independent claim, but also because of the additional features of the invention they define. In view of the foregoing, the Examiner is respectfully requested to reconsider and withdraw this rejection.

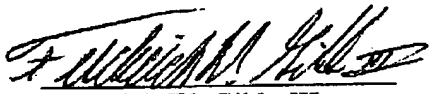
## II. Formal Matters and Conclusion

With respect to the rejections to the claims, the claims have been amended, above, to overcome these rejections. In view of the foregoing, Applicants submit that claims 1-21, all the claims presently pending in the application, are patentably distinct from the prior art of record and are in condition for allowance. The Examiner is respectfully requested to pass the above application to issue at the earliest possible time.

Should the Examiner find the application to be other than in condition for allowance, the Examiner is requested to contact the undersigned at the local telephone number listed below to discuss any other changes deemed necessary.

Please charge any deficiencies and credit any overpayments to Attorney's Deposit Account Number 09-0456.

Respectfully submitted,



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